IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Zbiciak	Art Unit: 2124
Serial No.: 09/703,034	Examiner: Chat C. Do
Filed: October 31, 2000	Docket: TI-30553
	Conf. No.: 8913

For: MICROPROCESSOR WITH ROUNDING DOT PRODUCT INSTRUCTION

Appeal Brief under 37 C.F.R. §41.37

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is Appellant's Appeal Brief filed pursuant to 37 C.F.R. §41.37 and the Notice of Appeal filed January 15, 2008.

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Real Party in Interest

The real party in interest in this application is Texas Instruments Incorporated, a corporation of Delaware with its principle place of business in Dallas, Texas. An assignment to Texas Instruments Incorporated is recorded at 011536 and frames 0374 and 0375.

Related Appeals and Interferences

There are no appeals of interferences related to this appeal in this application.

Status of the Claims

Claims 13 and 25 to 29 are rejected and subject to this appeal. No claims are allowed.

Status of Amendments Filed After Final Rejection

The ADVISORY ACTION of January 15, 2008 stated that the Amendment after Final Rejection filed October 8, 2008 would be entered upon filing this appeal.

Summary of Claimed Subject Matter

The subject matter of independent claims 13 and 25 is disclosed in the application as follows:

Claim 13	Disclosure
A digital system having a microprocessor operable to execute a rounding dot product instruction, wherein the microprocessor comprises:	digital system: Figure 1 - page 7, lines 3 to 6 microprocessor: 1 - page 7, line 16 to page 8, line 29 rounding dot product instruction: Figures 3A and 3B - page 16, line 6 to page 19, line 26

storage circuitry for holding pairs of elements;	storage circuitry: 20a - page 7, lines 24 to 25; 20b - page 8, lines 4 to 5
a multiply circuit connected to receive a first number of pairs of elements from the storage circuitry in a first execution phase of the microprocessor responsive to the dot product instruction, the multiply circuit comprising a plurality of multipliers equal to the first number of pairs of elements;	multiply circuit: MPY0 and MPY1 Figure 4 - page 20, lines 15 to page 21, line 22; MPY0 and MPY1 Figure 5 - page 24, lines 3 and 4; MPY0 and MPY1 Figure 6 - page 25, lines 17 to 19
an adder/subtractor circuit having a plurality of inputs each connected to receive a corresponding one of the plurality of products from the plurality of multipliers and a mid-position carry input to a predetermined bit for mid-position rounding responsive to the rounding dot product instruction; and	adder/subtractor circuit: 420 - page 22, lines 4 to 20; 520 - page 24, line 22 to page 25, line 2; 620 - page 26, lines 15 to 26 mid-position carry input: MRND Figure 4 - page 22, lines 21 to 28; MRND Figure 5 - page 25, lines 3 to 10; MRND Figure 6 - page 25, line 27 to page 27, line 5
a shifter connected to receive an output of the adder/subtractor circuit, the shifter operable to shift a selected amount in response to the rounding dot product instructions.	shifter: 440 - page 23, lines 8 to 10; 540 - page 25, lines 11 to 14

Claim 25	Disclosure
A data processing apparatus comprising:	digital system: Figure 1, page 7, lines 3 to 6
a first multiply circuit having first and second inputs and an output, said first multiply circuit operable in response to a dot product instruction to multiply data received at said first and second inputs and generate a first product at said output;	first multiply circuit: MPY0 Figure 4 - page 20, lines 15 to page 21, line 22; MPY0 Figure 5 - page 24, lines 3 and 4; MPY0 Figure 6 - page 25, lines 17 to 19

a second multiply circuit having first and second inputs and an output, said second multiply circuit operable in response to a dot product instruction to multiply data received at said first and second inputs and generate a second product at said output;	second multiply circuit: MPY1 Figure 4 - page 20, lines 15 to page 21, line 22; MPY1 Figure 5 - page 24, lines 3 and 4; MPY1 Figure 6 - page 25, lines 17 to 19
an adder/subtractor circuit having first and second inputs, a mid-position carry input to a predetermined bit and an output, said first input receiving said first product from said first multiply circuit, said second input receiving said second product from said second multiply circuits, said adder/subtractor circuit operable in response to said dot product instruction to arithmetically combine said first and second products and a "1" input at said mid-position carry input of said predetermined bit thereby forming a mid-position rounded sum; and	adder/subtractor circuit: 420 - page 22, lines 4 to 20; 520 - page 24, line 22 to page 25, line 2; 620 - page 26, lines 15 to 26 mid-position carry input: MRND Figure 4 - page 22, lines 21 to 28; MRND Figure 5 - page 25, lines 3 to 10; MRND Figure 6 - page 25, line 27 to page 27, line 5
a shifter connected to receive said mid-position rounded sum of the adder/subtractor circuit, the shifter operable to shift said mid-position rounded sum a predetermined amount in response to said dot product instruction.	shifter: 440 - page 23, lines 8 to 10; 540 - page 25, lines 11 to 14

This application includes no "means plus function" claims and no "step plus function" claims.

Grounds for Rejection to be Reviewed on Appeal

1. Claim 28 was rejected under 35 U.S.C. 112, second paragraph, as indefinite for failing to particularly point out and

distinctly claim the subject matter which applicant regards as the invention.

2. Claims 13 and 25-29 were rejected under 35 U.S.C. 101 as directed to non-statutory subject matter.

3. Claim 13 was rejected under 35 U.S.C. 103(a) as made obvious by the combination of Saishi et al. U.S. Patent No. 6,167,419 and Pitsianis et al. U.S. Patent Application Publication No. 2003/00088601.

4. Claims 25-27 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Saishi et al. U.S. Patent No. 6,167,419 and Peleg et al. U.S. Patent No. 6,385,634.

Arguments

1. Claim 28 was rejected under 35 U.S.C. 112, second paragraph, as indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The FINAL REJECTION states that limitations to the first and second Q shifters are incomplete.

The ADVISORY ACTION of January 15, 2008 stated that the amendment after final rejection submitted October 8, 2007 would be entered but failed to state whether this amendment cured this rejection.

Claim 28 is proper under 35 U.S.C. 112. Claim 28 was amended to explicitly state that the first and second Q shifters operate "responsive to the rounding dot product instruction." The Applicant submits that by this amendment the limitations are complete. Accordingly, claim 28 is proper under 35 U.S.C. 112.

2. Claims 13 and 25 to 29 were rejected under 35 U.S.C. 101 as directed to non-statutory subject matter. The FINAL REJECTION states that claims 13 and 25 to 29 cite a system and apparatus for performing a dot product in accordance with a mathematical algorithm, merely disclosing steps/components for performing a dot product without further disclosing a practical/physical application or a useful and tangible result. The FINAL REJECTION further states the claims preempt every substantial practical application of the idea embodied by the claim and there is no cited limitation in the claims that breathes sufficient life and meaning into the preamble so as to limit it to a particular practical application rather than being so broad and sweeping as to cover every substantial practical application of the idea embodied therein.

Claims 13 and 25 to 29 recite statutory subject matter. Independent claim 13 recites "A digital system." Independent claim 25 recites "A data processing apparatus." Thus the claims in this

application are directed to a machine which is of a class of subject matter eligible for patent protection. The application teaches a concrete, useful and tangible application for the data processing apparatus recited in independent claims 13 and 25. This application states at page 2, lines 10 to 17:

> "Special-purpose microprocessors, in contrast, are designed to provide performance improvement for specific predetermined arithmetic and logical functions for which the user intends to use the microprocessor. By knowing the primary function of the microprocessor, the designer can structure the microprocessor architecture in such a manner that the performance of the specific function by the special-purpose microprocessor greatly exceeds the performance of the same function by a general-purpose microprocessor regardless of the program implemented by the user."

Thus this portion of the application states that a special-purpose microprocessor such as disclosed and claimed may implement a specific function with greater performance than a general-purpose microprocessor. This application further state at page 19, lines 3 to 23:

> "In this embodiment, rounding at bit 16 of the 32-bit combined product with a rounding value of 0x8000 (2^{15}) and right shifting sixteen bits is performed in order to reduce processing time required for applications such as IDCT. The inventor of the present invention discovered that source code written for applications such as IDCT in the known C programming language often contains a sequence of instructions such as the following:

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"Q1 = (F1*C7 - F7*C1 + 0x8000) >> 16;
"Q0 = (F5*C3 - F3*C5 + 0x8000) >> 16;
"S0 = (F5*C5 + F3*C3 + 0x8000) >> 16;
"S1 = (F1*C1 + F7*C7 + 0x8000) >> 16;
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> "Advantageously, by using the dot product instructions of the present invention, the C-code sequence above can be directly replaced with a sequence similar to the following, for example, to reduce instruction count and improve processing

performance:

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"Q1    = _dotpnrsu2(F17, C71);
"Q0    = _dotpnrsu2(F53, C35);
"S0    = _dotprsu2 (F53, C53);
"S1    = _dotprsu2 (F17, C17);"
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Thus this application teaches that the invention reduces the number of instructions needed to perform a known C code implementation of an Inverse Discrete Cosine Transform (IDCT) function. As noted in the application at page 2, line 25 to page 3, line 3, the IDCT function is one of a set of problems for with a digital signal processor is suitable for "real-time applications such as image and speech processing." Thus this application teaches a concrete use of an embodiment of the data processing apparatus recited in these claims.

The Applicants submit that the utility asserted in the above quoted portion of the application is substantial and specific. These claims recite a digital system and a data processing apparatus and the asserted utility is a type of data processing which can be preformed by a digital system. The asserted utility employs multipliers MPY 0 and MPY 1, adder 420 and shifter 440 illustrated in Figure 4 in a manner ordinarily expected of such parts by one skilled in the art. Accordingly this asserted utility is more than an insubstantial, nonspecific or throw-away utility.

Claim 13 recites that the adder/subtractor circuit includes "a mid-position carry input to a predetermined bit for mid-position rounding responsive to the rounding dot product instruction." Claim 25 similarly recites that the adder/subtractor circuit includes "a mid-position carry input to a predetermined bit" and "operable in response to said dot product instruction to arithmetically combine said first and second products and a '1' input at said mid-position carry input of said predetermined bit thereby forming a mid-position rounded sum." The Applicant urges

that each such limitation "breathes sufficient life and meaning into the preamble so as to limit it to a particular practical application." The Applicants urge that these are limitations upon the particular hardware and are particularly adapted to the rounding dot product instruction of this application. Thus this application is to a particular, concrete machine and do not attempt to preempt a mathematical algorithm.

These claims are statutory subject matter because the claimed machine produces a useful, tangible and concrete result. This asserted utility is tied to particular machine limitations. Thus the asserted utility is tangible. The Applicants urge that the use of the claimed machine is repeatable. The claimed machine will provide the same result upon repeated use. Thus this use is concrete. Accordingly, the claims of this application have a practical application with a useful, tangible and concrete result and are thus statutory subject matter.

The above quoted portion of the FINAL REJECTION indicates that the Examiner believes claims 13 and 25 to 29 preempt one of the 35 U.S.C. 101 judicial exceptions. Section IV.C.3 of the "Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility" of the OFFICIAL GAZETTE of November 22, 2005 instruct the Examiner to make a determination whether the claimed invention preempts an abstract idea, law of nature, or natural phenomenon (Sec. 101 judicial exceptions). In particular Section IV.C.3 of the Interim Guidelines state:

> "If an examiner determines that the claimed invention preempts a Sec. 101 judicial exception, the examiner must identify the abstraction, law of nature, or natural phenomenon and explain why the claim covers every substantial practical application thereof."

The Applicants respectfully submit that the FINAL REJECTION includes only an unsupported statement and fails to make this

identification. The Applicants urge that claims 13 and 25 to 29 define a machine and do not attempt to preempt a Sec. 101 judicial exception. The Applicant urges that the rounding dot product operation of this invention could be performed by a properly programmed general-purpose computer. In particular, the combined addition or subtraction and rounding recited as carried out simultaneously in the adder/subtractor circuit recited in claims 13 and 25 could be carried out in two operations: a first addition or subtraction of the products; followed by addition of an appropriate quantity for the rounding. These two operations could be performed using two circuits in cascade or by two sequential operations in a single adder/subtractor. The Examiner has cited the combination of Saishi et al and Pitsianis et al as capable of performing the rounding dot product operation of this invention. The Applicant understands this combination to use adder/subtrators 623 and 625, 723 and 725, 1723 and 1725, or 1823 and 1825 to combine products and respective round and select circuits 627, 727, 1727 or 1827 to perform the rounding. The FINAL REJECTION fails to explain how granting claims 13 and 25 preempt practicing the dot product algorithm in the manner of these examples. Accordingly, grant of a patent on this application would not "cover every substantial practical application of the idea embodied" in claims 13 and 25 to 29. If the Examiner continues to believe that claims 13 and 25 to 29 are non-statutory because they preempt a Sec. 101 judicial exception, the Applicant urges the Examiner to make the identification of the above quoted portion of the Interim Guidelines. The Applicant requests an explanation why the examples of other manners of practicing a dot product multiply are not feasible. In the absence of such a showing, claims 13 and 25 to 29 recite statutory subject matter.

In response to prior arguments that the current claims are apparatus claims and not method claims, the FINAL REJECTION states

at page 10, lines 4 to 6:

> "The examiner respectfully submits that the claims are still directed to non-statutory subject matter under current language. The claims only disclose the general circuit components for performing basic mathematical operations."

The Applicant respectfully urges that this is incorrect. A claim to a machine would be statutory subject matter even if its only practical use were in performing a mathematical operation. It is axiomatic that an assembly of general circuit components can be arranged and connected in a novel, unobvious manner. Such an assembly would be statutory subject matter. The Applicant urges that the recited "general circuit components" in claims 13 and 25 to 29 are so arranged and connected as to constitute statutory subject matter.

The ADVISORY ACTION states at the continuation of paragraph 11, lines 6 to 11:

> "The examiner respectfully submits that the claims are still directed to non-statutory subject matter because of the following reasons: first, claims only disclose a mathematical algorithm (e.g. in this case the rounding dot product algorithm) that is implemented in a general hardware components without disclosing or addressing any practical application as required; second, with only the mathematical algorithm in these claims would preempt substantially all the practical applications of utilizing the algorithm which is the dot product. All the explanations of the practical applications in pages 7-8 are not cited in the claims and further the machine claim disclosed a purely methamtical (sic) operation would consider to be as non-statutory subject matter."

The Applicant disputes that the claims "only disclose a mathematical algorithm." Claim 13 recites the physical elements of storage circuitry, a multiply circuit, an adder/subtractor circuit and a shifter. Claim 25 recites the physical elements of a first

multiply circuit, a second multiply circuit, an adder/subtractor circuit and a shifter. Thus these claims do not "only disclose a mathematical algorithm." The Examiner has not substantiated how the current claims "preempt substantially all the practical applications of utilizing the algorithm." Previous responses by the Applicant and this APPEAL BRIEF propose examples of how the rounding dot product algorithm can be practiced without using the claimed subject matter. The Examiner has not refuted these examples of non-preemption. The comment that the practical applications "are not cited in the claims" is inappropriate. The "Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility" require that "the claimed invention as a whole must accomplish a practical application." This requirement is different than requiring the claims recite the practical application. In this application the machine elements recited in claims 13 and 25 accomplish a practical application as set forth in the above quoted portion of the specification. Accordingly, claims 13 and 25 present statutory subject matter.

Claim 28 includes additional statutory subject matter. Claim 28 recites the machine elements of a first Q shifter and a second Q shifter. Each of these machine elements include particularly recites connections to element of base claim 25 and particularly recited functions. Thus claim 28 does not recite or attempt to preempt a mathematical algorithm. Accordingly, claim 28 presents statutory subject matter.

Claim 29 includes additional statutory subject matter. Claim 29 includes a limitation upon the machine elements of the first multiply circuit, the second multiply circuit, the adder/subtractor circuit and the shifter. This limitation requires that these elements operate using a particular number representation format. Those skilled in the art would realize that this limitation requires a different construction of the recited machine elements.

Thus claim 29 does not recite or attempt to preempt a mathematical algorithm. Accordingly, claim 29 presents statutory subject matter.

Claim 29 recites further additional statutory subject matter. Claim 29 recites a further machine element in the carry save adder. Claim 29 recites particular connections for this carry save adder and particular machine functions. Thus claim 29 does not recite or attempt to preempt a mathematical algorithm. Accordingly, claim 29 presents statutory subject matter.

3. Claim 13 was rejected under 35 U.S.C. 103(a) as made obvious by the combination of Saishi et al U.S. Patent No. 6,167,419 and Pitsianis et al. U.S. Patent Application Publication No. 2003/00088601.

Claim 13 recites subject matter not made obvious by the combination of Saishi et al and Pitsianis et al. Claim 13 recites "an adder/subtractor circuit having a plurality of inputs each connected to receive a corresponding one of the plurality of products from the plurality of multipliers." The FINAL REJECTION cites elements 506 to 508 illustrated in Figure 5 of Saishi et al as making obvious the claimed adder/subtractor circuit. The Applicant respectfully submits that these elements of Saishi et al do not make obvious the claimed adder/subtractor circuit because Saishi et al teaches rounding at a different place than recited in claim 13. Saishi et al states at column 12, lines 16 to 23:

> "numeral 506 designates a first subproduct addition means as a component of the multiplication means 503, numeral 507 designates an intermediate register for temporarily storing an intermediate result from the first subproduct addition means 506, numeral 508 designates a second subproduct addition means for adding the output of the intermediate register 507 and used as a component of the multiplication means 503, numeral 509 designates a multiplication result obtained after rounding and used as the output of the second subproduct addition means

508"

Thus Saishi et al clearly states that elements 506 to 508 cannot be the claimed adder/subtractor circuit combining plural products but are part of the multiplication means 503. This portion of Saishi et al teaches that multiplication means 503 produces a product output at element 509. Claim 13 recites that the adder/subtractor circuit receives product outputs at its inputs. These product outputs correspond to element 509 taught in Figure 5 of Saishi et al. However, Saishi et al teaches no supply of this product 509 to an adder/subtractor circuit. Saishi et al teaches supply of product 509 to switching means 520 and then to barrel shifter 510 and shift and multiplication results register 511. Thus Saishi et al teaches rounding during subproduct addition within a single multiplication rather than while adding or subtracting plural products as recited in claim 13. Combining the teaching of Pitsianis et al with the teaching of Saishi et al would result in plural multipliers each rounding as taught in Saishi et al and adding the rounded products as taught in Pitsianis et al, perhaps eliminating the rounding following the addition taught in Pitsianis et al. Accordingly, claim 13 is allowable over the combination of Saishi et al and Pitsianis et al.

Rounding in the adder/subtractor circuit of claim 13 is unobvious over the combination of Saishi et al and Pitsianis et al. Pitsianis et al teaches production of two products but does not teach a single adder/subtractor circuit combining these two products and rounding as recited in claim 13. Figure 6 of Pitsianis et al teaches combining products in subtractor 623 and adder 625, and rounding the selection and rounder circuit 627. Figure 7 of Pitsianis et al teaches combining products in adder 723 and subtractor 725, and rounding in selection and rounder circuit 727. Figure 17 of Pitsianis et al teaches combining products in

adder block 1723 and adder block 1725, and rounding in selection and rounder circuit 1727. Figure 18 of Pitsianis et al teaches combining products in adder block 1823 and adder block 1825, and rounding in selection and rounder circuit 1827. The Applicants respectfully submit that both Saishi et al and Pitsianis et al teach rounding in a portion of the circuit different from that recited in claim 13. As noted above, Saishi et al teaches rounding as part of subproduct addition within a single multiplication resulting in a single rounded product. Pitsianis et al teaches a separate circuit or operation applied after combining plural products. In contrast, claim 13 recites both combining the plural products and rounding in the claimed adder/subtractor circuit. Accordingly, claim 13 is not made obvious by the combination of Saishi et al and Pitsianis et al.

Claims 13 recites further subject matter not made obvious by the combination of Saishi et al and Pitsianis et al. Claim 13 recites the adder/subtractor circuit includes "a mid-position carry input to a predetermined bit for mid-position rounding responsive to the rounding dot product instruction." This application combines operations normally requiring two hardware circuits into a single hardware circuit. The two combined operations are the sum/difference of the products and rounding the result. Those skilled in the art would understand the claimed adder/subtractor circuit to include a chain of plural bit circuits. Each bit circuit receives a carry input from the immediately prior bit circuit and supplies a carry output to the immediately following bit circuit. As recited in claim 13, rounding results when an active carry signal is supplied to the mid-position carry input of this bit circuit chain. Even if first subproduct addition means 506 of Saishi et al is regarded as the claimed adder/subtractor circuit, Saishi et al fails to teach this use of a mid-position carry input to a predetermined bit for the recited rounding.

Saishi et al states at column 8, lines 27 to 35:

> "When the range indicated by the bit range 804 of the multiplication result 803 is desired to be cut out, and when it is assumed that the predetermined rounding position 811 is basically located at the mth bit from the least significant bit in consideration of the fact that a shift count required for a shift operation for cutting out is indicated by a right shift 809 of kbits, a signal having '1' at the (m+k)th bit is generated as the rounding signal. In other words, the rounding position is shifted to the left by k bits."

This clearly teaches that the rounding position is selected by the rounding generator generating a rounding signal shifted to correspond to the later shift of the rounded product. One skilled in the art would understand the recited "shifted to the left by k bits" to be a multibit signal having 0's shifted into the k least significant bits to place a single 1 bit in the desired rounding position. Figures 1 to 5 of Saishi et al show this rounding signal applied to a normal data input of an addition means. Saishi et al never states that the rounding signal is input to "a mid-position carry input to a predetermined bit" as recited in claim 13. The FINAL REJECTION fails to cite any portion of Saishi et al as making obvious the recited mid-position carry input to a predetermined bit. One skilled in the art would understand Saishi et al to teach supply of a multi-bit rounding signal to an ordinary multi-bit data input of the adder. The left shifted 1 generated by the rounding signal generator is thus supplied to a data input and not to the carry input of a predetermined bit recited in claim 13. Thus Saishi et al teaches achieving the same result of this invention using a different method step or different apparatus. While the FINAL REJECTION states that this is disclosed in Saishi et al, in fact neither addition means 109, addition means 209, first subproduct addition means 306, first subproduct addition means 406, nor first subproduct addition means 506 illustrate the

"mid-position carry input to a predetermined bit" recited in claim 13. The description of these parts in Saishi et al indicates that the rounding signal is supplied to a data input of the corresponding addition means. Saishi et al states at column 6, lines 11 to 14:

> "The multiplication result 104 and the rounding signal 106 are input to the addition means 109, and the addition means 109 outputs the multiplication result 110 obtained after rounding."

Saishi et al states at column 10, lines 50 to 53:

> "The subproducts 305 and the rounding signal 315 are added by the first subproduct addition means 306."

This disclosure with the teaching of Saishi et al that the rounding signal is "shifted to the left by k bits" makes clear that the rounding signal is supplied to each bit of a multi-bit input of addition means 109, addition means 209, first subproduct addition means 306, first subproduct addition means 406 and first subproduct addition means 506 rather than the "mid-position carry input to a predetermined bit" recited in claim 13. The FINAL REJECTION does not allege that Pitsianis et al makes obvious this subject matter. Accordingly, claim 13 is not made obvious by the combination of Saishi et al and Pitsianis et al.

4. Claims 25 to 27 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Saishi et al U.S. Patent No. 6,167,419 and Peleg et al U.S. Patent No. 6,385,634.

Claim 25 recites subject matter not made obvious by the combination of Saishi et al and Peleg et al. Claim 25 recites "an adder/subtractor circuit having a first and second inputs" and "said first input receiving said first product from said first

multiply circuit, said second input receiving said second product from said second multiply circuits." The FINAL REJECTION cites elements 506 to 508 illustrated in Figure 5 of Saishi et al as making obvious the claimed adder/subtractor circuit. The Applicant respectfully submits that these elements of Saishi et al do not make obvious the claimed adder/subtractor circuit because Saishi et al teaches rounding at a different place than recited in claim 25. Saishi et al states at column 12, lines 16 to 23:

> "numeral 506 designates a first subproduct addition means as a component of the multiplication means 503, numeral 507 designates an intermediate register for temporarily storing an intermediate result from the first subproduct addition means 506, numeral 508 designates a second subproduct addition means for adding the output of the intermediate register 507 and used as a component of the multiplication means 503, numeral 509 designates a multiplication result obtained after rounding and used as the output of the second subproduct addition means 508"

Thus Saishi et al clearly states that elements 506 to 508 cannot be an adder/subtractor circuit adding pairs of products but are part of the multiplication means 503. This portion of Saishi et al teaches that multiplication means 503 produces a product output at element 509. Claim 25 recites that the adder/subtractor circuit receives product outputs at its inputs. These product outputs correspond to element 509 taught in Figure 5 of Saishi et al. However, Saishi et al teaches no supply of this product 509 to an adder/subtractor circuit. Saishi et al teaches supply of product 509 to switching means 520 and then to barrel shifter 510 and shift and multiplication results register 511. Thus Saishi et al teaches rounding during subproduct addition within a single multiplication rather than while adding or subtracting plural products as recited in claim 25. Combining the teaching of Peleg et al with the teaching of Saishi et al would result in plural multipliers each

rounding as taught in Saishi et al and adding the rounded products as taught in Peleg et al. Accordingly, claim 25 is allowable over the combination of Saishi et al and Peleg et al.

Rounding in the adder/subtractor circuit of claim 25 is unobvious over the combination of Saishi et al and Peleg et al. Peleg et al teaches production of two products but does not teach a single adder/subtractor circuit combining these two products and rounding as recited in claim 25. Figure 8 of Peleg et al teaches combining products in adder/subtractors 850 and 851. The Applicants respectfully submit that Saishi et al teaches rounding in a portion of the circuit different from that recited in claim 25. As noted above, Saishi et al teaches rounding as part of subproduct addition within a single multiplication resulting in a single rounded product. Peleg et al fails to teach any circuit in Figure 8 for rounding. In contrast, claim 25 recites both combining the plural products and rounding in the claimed adder/subtractor circuit. Accordingly, claim 25 is not made obvious by the combination of Saishi et al and Peleg et al.

Claims 25 recites further subject matter not made obvious by the combination of Saishi et al and Peleg et al. Claim 25 recites the adder/subtractor circuit includes "a mid-position carry input to a predetermined bit for mid-position rounding responsive to the rounding dot product instruction." This application combines operations normally requiring two hardware circuits into a single hardware circuit. The two combined operations are the sum/difference of the products and rounding the result. Those skilled in the art would understand the claimed adder/subtractor circuit to include a chain of plural bit circuits. Each bit circuit receives a carry input from the immediately prior bit circuit and supplies a carry output to the immediately following bit circuit. As recited in claim 25, rounding results when an active carry signal is supplied to the mid-position carry input of

this bit circuit chain. Even if first subproduct addition means 506 of Saishi et al is regarded as the claimed adder/subtractor circuit, Saishi et al fails to teach this use of a mid-position carry input to a predetermined bit for the recited rounding. Saishi et al states at column 8, lines 27 to 35:

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This clearly teaches that the rounding position is selected by the rounding generator generating a rounding signal shifted to correspond to the later shift of the rounded product. One skilled in the art would understand the recited "shifted to the left by k bits" to be a multibit signal having 0's shifted into the k least significant bits to place a single 1 bit in the desired rounding position. Figures 1 to 5 of Saishi et al show this rounding signal applied to a normal data input of an addition means. Saishi et al never states that the rounding signal is input to "a mid-position carry input to a predetermined bit" as recited in claim 25. The FINAL REJECTION fails to cite any portion of Saishi et al as making obvious the recited mid-position carry input to a predetermined bit. One skilled in the art would understand Saishi et al to teach supply of a multi-bit rounding signal to an ordinary multi-bit data input of the adder. The left shifted 1 generated by the rounding signal generator is thus supplied to a data input and not to the carry input of a predetermined bit recited in claim 25. Thus Saishi et al teaches achieving the same result of this invention using a different method step or different apparatus. While the

FINAL REJECTION states that this is disclosed in Saishi et al, in fact neither addition means 109, addition means 209, first subproduct addition means 306, first subproduct addition means 406, nor first subproduct addition means 506 illustrate the "mid-position carry input to a predetermined bit" recited in claim 25. The description of these parts in Saishi et al indicates that the rounding signal is supplied to a data input of the corresponding addition means. Saishi et al states at column 6, lines 11 to 14:

> "The multiplication result 104 and the rounding signal 106 are input to the addition means 109, and the addition means 109 outputs the multiplication result 110 obtained after rounding."

Saishi et al states at column 10, lines 50 to 53:

> "The subproducts 305 and the rounding signal 315 are added by the first subproduct addition means 306."

This disclosure with the teaching of Saishi et al that the rounding signal is "shifted to the left by k bits" makes clear that the rounding signal is supplied to each bit of a multi-bit input of addition means 109, addition means 209, first subproduct addition means 306, first subproduct addition means 406 and first subproduct addition means 506 rather than the "mid-position carry input to a predetermined bit" recited in claim 25. The FINAL REJECTION does not allege that Peleg et al makes obvious this subject matter. Accordingly, claim 25 is not made obvious by the combination of Saishi et al and Peleg et al.

Claims 26 and 27 are allowable by dependence upon allowable claim 25.

Since there is no art rejection of claims 28 or 29 and these claims are statutory subject matter, claims 28 and 29 are allowable.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Reg. No. 28,527

CLAIMS APPENDIX

13. A digital system having a microprocessor operable to execute a rounding dot product instruction, wherein the microprocessor comprises:

storage circuitry for holding pairs of elements;

a multiply circuit connected to receive a first number of pairs of elements from the storage circuitry in a first execution phase of the microprocessor responsive to the dot product instruction, the multiply circuit comprising a plurality of multipliers equal to the first number of pairs of elements;

an adder/subtractor circuit having a plurality of inputs each connected to receive a corresponding one of the plurality of products from the plurality of multipliers and a mid-position carry input to a predetermined bit for mid-position rounding responsive to the rounding dot product instruction; and

a shifter connected to receive an output of the adder/subtractor circuit, the shifter operable to shift a selected amount in response to the rounding dot product instructions.

25. A data processing apparatus comprising:

a first multiply circuit having first and second inputs and an output, said first multiply circuit operable in response to a dot product instruction to multiply data received at said first and second inputs and generate a first product at said output;

a second multiply circuit having first and second inputs and an output, said second multiply circuit operable in response to a dot product instruction to multiply data received at said first and second inputs and generate a second product at said output;

an adder/subtractor circuit having first and second inputs, a mid-position carry input to a predetermined bit and an output, said first input receiving said first product from said first multiply

circuit, said second input receiving said second product from said second multiply circuits, said adder/subtractor circuit operable in response to said dot product instruction to arithmetically combine said first and second products and a "1" input at said mid-position carry input of said predetermined bit thereby forming a mid-position rounded sum; and

a shifter connected to receive said mid-position rounded sum of the adder/subtractor circuit, the shifter operable to shift said mid-position rounded sum a predetermined amount in response to said dot product instruction.

26. The data processing apparatus of claim 25, wherein:

said arithmetic combination of said first and second products is an arithmetic sum.

27. The data processing apparatus of claim 25, wherein:

said dot product instruction is a dot product with negate instruction; and

said arithmetic combination of said first and second products is a difference of said second product from said first product in response to said dot product with negate instruction.

28. The data processing apparatus of claim 25, further comprising:

a first Q shifter having an input receiving said first product from said first multiply circuit and an output supplying said first input to said adder/subtractor circuit, said first Q shifter shifting said first product an instruction specified number of bits responsive to the rounding dot product instruction; and

a second Q shifter having an input receiving said second product from said second multiply circuit and an output supplying said second input to said adder/subtractor circuit, said second Q

shifter shifting said second product said instruction specified number of bits responsive to the rounding dot product instruction.

29. The data processing apparatus of claim 25, wherein:

said first multiply generates said first product in a redundant sign/magnitude format;

said second multiply circuit generates said second product in said redundant sign/magnitude format;

said adder/subtractor circuit arithmetically combines said first and second products and said "1" input at said mid-position carry input forming said mid-position rounded sum in said redundant sign/magnitude format;

a shifter shifts said mid-position rounded sum in said redundant sign/magnitude format; and

said data processing apparatus further comprises a carry save adder to 2's complement converter having an input receiving said shifted mid-position rounded sum in said redundant sign/magnitude format and an output generating a corresponding normal coded format.

Evidence Appendix

None

Related Proceedings Appendix

None